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Effects of nonideal characteristics of substrate BJT on bandgap reference circuit

Rui Bai
Iowa State University

Effects of non-ideal characteristics of substrate BJT on bandgap reference circuits

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Rui Bai

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Randall Geiger, Major Professor

Degang Chen

Zhengdao Wang

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DEDICATION

To my family

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ABSTRACT

The non-ideal characteristics of bipolar junction transistors (BJT) on the performance of band gap reference circuits are investigated. It is shown that the base spreading resistance (BSR) of a substrate BJT along with its temperature dependence has a significant negative impact on the performance of voltage references. It is shown that the temperature-dependent forward current gain (β) also adversely affects reference performance. In a typical application in a bulk CMOS process, the base spreading resistance causes an increase in the reference output of about 1% and the temperature dependent β introduces an inflection point shift of around 30 °C. After calibration the TC changes by 25 ppm/°C.

Keywords—base spreading resistance; temperature dependent β; bandgap reference circuit;

CHAPTERS 1: INTRODUCTION

In many state of the art integrated circuits, an accurate voltage reference that has a low sensitivity to the supply voltage, low sensitivity to variable process and model parameters, and low sensitivity to temperature is required. The bandgap voltage of silicon is independent of supply voltage, nearly independent of temperature, and shows almost no dependence upon process. For these reasons, most accurate voltage references that are used today are designed to have an output voltage that is proportional to the bandgap voltage. These references are termed "bandgap references". The concept of a bandgap reference was introduced in the mid 1970's by Widlar [1,2] and since that time numerous variants of the design have appeared including [14]-[17] but the basic performance of the bandgap circuits is similar to that of the Widlar structure. Invariably bandgap references are designed to have an output voltage that is proportional to the bandgap voltage of silicon. Precision bandgap voltage reference outputs are essential building blocks in mixed-signal analog integrated circuits design. Bandgap reference circuits produce stable reference voltages, which are insensitive to variations in voltage supplies, process parameters, and temperature. Bandgap reference circuits are commonly used in many applications such as analog to digital data converters (ADC), digital to analog data converters (DAC) and power management ICs. The increasing demand of higher accuracy and complexities in IC applications put more and more stringent design requirements on bandgap reference circuits, in particular, in how they are affected by variations in supply voltages, process parameters, and temperature.

Based upon existing analytical and computer models, the temperature coefficient (defined in Sec 2.2) of several of the basic bandgap references is around 5ppm/^{o}C over a 100^{o}C operating range centered round an operating temperature of 300K. The measured performance of reported basic bandgap reference circuits is typically in the 20ppm/^{o}C range to over 120ppm/^{o}C range and some measurement results actually exceed this range. The discrepancy between measured results and theoretical analysis differ by a factor of between 4 and grater than 20. This discrepancy has plagued designers for over 3 decades [7], [15], [16]. The differences between measured performance and both analytical and simulation results must be attributable to model errors. In this thesis, further attention will be given to resolving the differences between simulated and measured results.

The components that comprise a bandgap circuit are basic and consist primarily of resistors, an operational amplifier, and either a diode or bipolar junction transistor. Some authors have focused on the non-ideal characteristics of the op amp, specifically input-referred offset voltage and the finite gain, but these factors are not sufficient to describe the differences between simulated and measured performance. In this work, emphasis will be placed on the effects of the non-ideal characteristics of the diodes or bipolar transistors. In this chapter the operating principles of bandgap reference circuits are discussed along with a summary of several of the different circuit structures used to implement bandgap references.

1.1 The basics of bandgap reference circuits

The I-V characteristics of the pn junction can be expressed as (1).

$$I_D(T) = I_S e^{\frac{V_D(T)}{V_t}} = \left(\tilde{J}_{SX} A \left[T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) e^{\frac{V_D(T)}{V_t}} \quad (1)$$

where m=-3/2 and $\tilde{J}_{SX}$ are process-dependent model parameters, A is the area of the junction, T is temperature in K, V_t is the thermal voltage (V_t=kT/q), and V_{G0} is the bandgap voltage. The bandgap voltage is a physical constant that is independent of process and is highly insensitive to temperature. Bandgap reference circuits are designed to express the bandgap voltage that appears in the model of a pn junction at the output.

Designing a circuit that expresses the deeply embedded bandgap voltage parameter at the output appears to be an arduous task. Most authors have rather approached the design of voltage references by obtaining a circuit with two outputs, one with a positive temperature coefficient and a second with a negative temperature coefficient with the goal of creating a weighted sum that has a zero temperature coefficient at the inflection point temperature. Following this approach, they then observed that some of these circuits have an output voltage that equals the bandgap voltage at the inflection point temperature. This approach will be followed in this chapter.

Thus, consider the generation of two voltages V_1 and V_2 with complementary temperature coefficients. The voltage reference output is defined as (2)

$$V_{REF} = aV_1 + bV_2 \quad (2)$$

where the a and b coefficients are independent of temperature. These coefficients are chosen in such way that at a temperature $T=T_{INF}$

$$\left.\frac{\partial V_{REF}}{\partial T}\right|_{T=T_{INF}} = a\left.\frac{\partial V_1}{\partial T}\right|_{T=T_{INF}} + b\left.\frac{\partial V_2}{\partial T}\right|_{T=T_{INF}} = 0 \quad (3)$$

At $T=T_{INF}$, the voltage reference has a zero temperature coefficient. Ideally this derivative will be small throughout a large temperature range around T_{INF}. If a and b are positive then the positive temperature coefficient (PTC) of the voltage V_1 and the negative temperature coefficient (NTC) of the voltage V_2 can be defined as (4) and (5), respectively.

$$PTC = \left.\frac{\partial V_1}{\partial T}\right|_{T=T_{INF}} > 0 \tag{4}$$

$$NTC = \left.\frac{\partial V_2}{\partial T}\right|_{T=T_{INF}} < 0 \tag{5}$$

Among various device parameters in semiconductor technologies, some characteristics of the pn junction and/or the bipolar junction transistor have proven to be particularly useful for designing simple circuits that can provide positive and negative temperature coefficients [18]. Due to these properties, the pn junction and/or bipolar transistors serve as key building blocks for the design of bandgap reference circuits.

The voltage across a diode or a diode-connected bipolar transistor under constant current bias has a negative temperature coefficient. The fundamental operation of a bipolar transistor is shown in (6).

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{6}$$

$$V_T = \frac{kT}{q} \tag{7}$$

After manipulation (6), we can find the expression of the base-emitter voltage of bipolar transistors, which is shown in (8). The saturation current is described in (9), where $m = -3/2, m_1 = 5/2$ and the bandgap energy of silicon is V_{G0}; $V_{G0} = 1.12eV$. b is a

proportionality factor. In (10), $V_{BE} \approx 750mV$ when $T = 300K$, therefore $\frac{\partial V_{BE}}{\partial T} \approx -1.5mV/K$ which is a negative value and it serves as the negative temperature coefficient.

$$V_{BE} = V_T \ln(\frac{I_C}{I_S}) \tag{8}$$

$$I_S = bT^{m_1} e^{-V_{G0}/kT} \tag{9}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - m_1 V_T - V_{G0}/q}{T} \tag{10}$$

If two bipolar transistors bear different currents with a fixed ratio, then a voltage that exhibits a positive temperature coefficient can be found as the difference between the two base-emitter voltages. It can be showed as (11), where n is the current ratio between the two bipolar transistors. Both n and k/q are positive, therefore $\frac{\partial \Delta V_{BE}}{\partial T}$ in (12) is a positive value. It serves as the positive temperature coefficient.

$$\Delta V_{BE} = V_T \ln(n) \tag{11}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln(n) \tag{12}$$

With the negative and positive temperature coefficients obtained above, bandgap reference circuits can be developed. Different types of bandgap reference circuits are shown in Section 1.2.

1.2 Architectures of bandgap reference circuits

Since the mid 1970's, bandgap references circuits have been widely used in analog IC design. Widlar published some of the first papers on the subject in 1969 and 1971 while

working at National Semiconductor [2]. A third early paper on the topic is that of Brokaw in 1974, who was working at Analog Devices [15].

Fig.1 shows four different basic architectures of bandgap reference circuits. Start-up circuits are required for these references but do not affect the basic voltage-temperature characteristics under normal operation so are not shown in the figure to reduce notational complexity. Fig. 1 (a) is known as the Brokaw bandgap reference circuit [14]. Fig. 1 (b) is a low-voltage bandgap reference circuit [15]. The Kuijk bandgap reference circuit is shown in Fig. 1 (c) [16]. The voltage reference circuit in Fig. 1 (d) was introduced by Zhu [17]. It includes two op-amps, which will increase the power consumption and the design complexity.

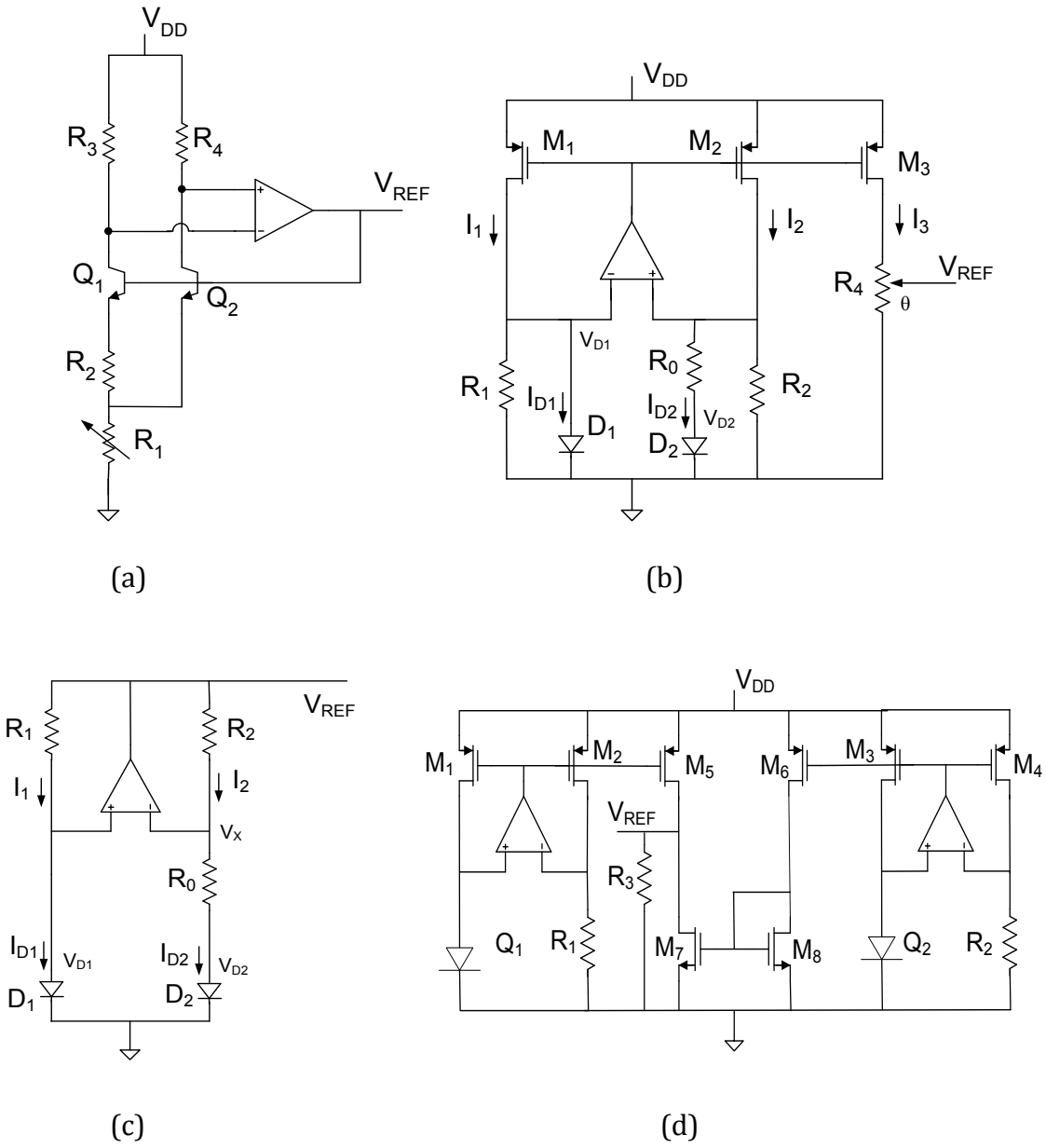
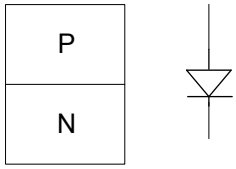


Figure 1 Architecture of bandgap reference circuits (a) Brokaw [14] (b) Low-voltage [15] (c) Kuijk [16] (d) voltage reference output of Zhu [17]

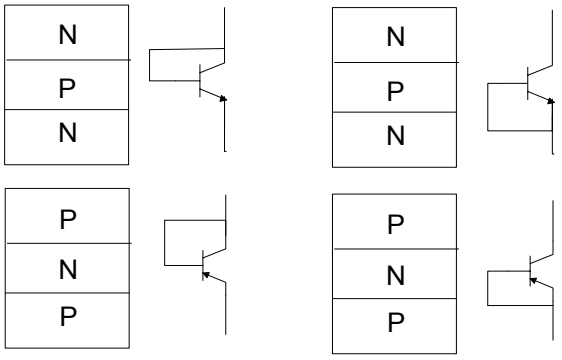
1.3 RESEARCH OBJECTIVE

The circuits shown Fig. 1(b), Fig. 1(c) and Fig. 1(d) and most other bandgap circuits employ two diodes. Unfortunately a good diode is seldom available in most basic CMOS processes. However, in most processes, a parasitic pnp or a parasitic npn stack is

available. These three-diffusion stacks form parasitic bipolar transistors. By connecting the middle diffused region to either the upper or lower diffusion in these parasitic bipolar transistors, a “diode-connected transistor” can be formed. Fig. 2 shows a junction diode and diode-connected transistors.



(a) Junction diode



(b) Diode-connected transister

Figure 2 Junction diode and diode-connected transistor

The I-V characteristics of a diode-connected transistor and the temperature characteristics of the diode-connected transistor are similar to those of a basic pn junction. Consequently, available parasitic diode-connected transistors are widely used in the design of integrated bandgap circuits. But there are some characteristics of the diode-connected transistor that differ from those of a basic pn junction as well. One is the dc current gain, often termed the transistor β that does not exist in a pn junction. Related is the effect of current crowding in the base region due to the internal base-spreading resistance. A third

is the series base resistance needed to make electrical contact with the base region of the parasitic bipolar devices.

Correspondingly, the measured performance of bandgap circuits often differs considerably from that analytically predicted using an ideal pn junction and often differs considerably from that predicted by computer simulations using either a pn junction or a diode-connected transistor [4], [16], [5]. Differences between simulated and measured performance makes it difficult for designers to draw closure in the design process and makes it difficult to do performance optimization on a design. There has been some work done on modeling of non-ideal effects on the performance of bandgap circuits. Some authors have focused on the finite dc gain of the op amp [10], [13], some have focused on the offset voltage of the op amp [7] ~ [11], [24] and some have looked at the effects of the temperature coefficients of the resistors in the circuit [6], [11], [24]. Though these effects all contribute to some degradation in performance, they can and are naturally included in good simulations but even when these effects are included, there is still a substantial discrepancy between simulated or predicted results and experimental results [7],[12],[24]. It can be concluded that there must be some additional non-ideal effects that are contributing to a discrepancy between measured and simulated results. Since the non-ideal effects of the resistors and operational amplifiers have been well studied, non-ideal characteristics of the diode or diode-connected resistors are likely the major contributor to these discrepancies.

The effects of non-ideal characteristics of the diode-connected bipolar transistor on the performance of bandgap circuits are seldom discussed and some of these non-ideal characteristics are not easily included in simulations of extracted circuits. However, the

overall effects the non-ideal characteristics of the diode-connected transistor have on bandgap voltage references can be significant. Especially in modern analog design where the performance requirements of voltage references are often stringent, it is particularly important to have good correlation between measured results and simulation results.

The electrical characteristics of a bipolar transistor are strongly affected by the diffused base region. A large area bipolar transistor contains non-negligible parasitic resistance in the base region. This is known as the base-spreading resistance. The effective local base-emitter voltage varies with position throughout the base region and causes current crowding, which is the non-homogenous distribution of current density through the base region. Because of the exponential relationship between collector current and base-emitter voltage, the effects of current crowding on the electrical characteristics of a bipolar transistor can be significant.

In this work, the non-ideal characteristics of bipolar junction transistors on the performance of bandgap reference circuits are investigated with a goal of developing models of bandgap circuits that more accurately predict their actual performance. It is shown that the base spreading resistance of a substrate bipolar transistor along with its temperature dependence has a significant negative impact on the performance of voltage references. It is shown that the temperature-dependent forward current gain (β) also adversely affects reference performance.

In a typical application in a bulk CMOS process, the base spreading resistance causes an increase in the reference output of about 1% and the temperature dependent β introduces an inflection point shift of around 30 °C. After calibration, the TC of one bandgap reference changes by 25 ppm/°C in a typical bulk CMOS process. Corresponding

changes, which may be larger or may be smaller in magnitude, are anticipated for other bandgap reference circuits and other bulk CMOS processes.

In a bulk CMOS process, parasitic vertical substrate bipolar transistors can be easily constructed and this substrate BJT can be used to create a diode-connected transistor needed in some bandgap circuits. The non-ideal characteristics of this substrate diode-connected bipolar transistor can cause inaccuracies in the voltage reference output. In a typical vertical substrate bipolar transistor, a well diffusion is used to create the base region of the transistor. This well region is both thick and relatively lightly doped. The characteristics of all bipolar transistors are strongly affected by the diffused base region. The base spreading resistance will cause a distributed base-emitter voltage drop in bipolar transistors and the collector current will vary due to these voltage changes.

Several non-ideal characteristics of a diode-connected transistor on the performance of a bandgap reference will be considered and strategies will be developed to quantify their effects. One strategy will be to develop a new model of the bipolar transistor, which can be used to model the effects of the base spreading resistance. This new bipolar model will be applied to the Kuijk bandgap reference from which we can see the effects of the base spreading resistance on the voltage reference output. It will be shown that the base spreading resistance affects the inflection point, the TC, and the magnitude of the reference output voltage.

A second strategy will focus on modeling the temperature dependence of the beta in a diode-connected bipolar transistor and determining the effects this has on the Kuijk bandgap reference circuit. It will be shown that the temperature-dependent beta will also impact both of the inflection point and the TC of voltage reference output.

A third strategy will focus on the temperature dependence of the resistors in the Kuijk bandgap reference circuit. These effects were considered in one specific structure by Vishal Gupta in [24]. It will be shown that the temperature coefficient variation of those resistors in the bandgap reference significantly impact the inflection point of the voltage reference output.

Finally, the calibration on the voltage reference output will be investigated. Local and global process variations and mismatch, offset voltages in the op amp, and package stress [6] will cause the inflection point to shift and the magnitude of the output to change. Local and global variations in resistors in particular, will cause a significant change in performance and are often dominant contributors to performance degradation. Due to the non-ideal characteristics in bipolar transistor and temperature dependence of the resistors, the voltage reference output will suffer temperature drift. Therefore, calibration has to be applied to the voltage reference output to improve the accuracy.

This thesis is organized as follows. A standard analysis of a common bandgap reference circuit is presented in Chapter 2. This is followed with a more rigorous analysis that includes non-ideal effects of both diode-connected transistors and resistors in Chapter 3. In Chapter 4, simulation results of a bandgap circuit are presented that include the nonideal effects of the diode-connected transistors and the resistors in the circuit. Calibration is discussed in Chapter 5.

CHAPTER 2: KUIJK BANDGAP REFERENCE

The Kuijk bandgap reference circuit is repeated in Fig. 3. This circuit was first discussed in 1973 [2]. Kuijk used two diodes to sense the variation of the temperature.

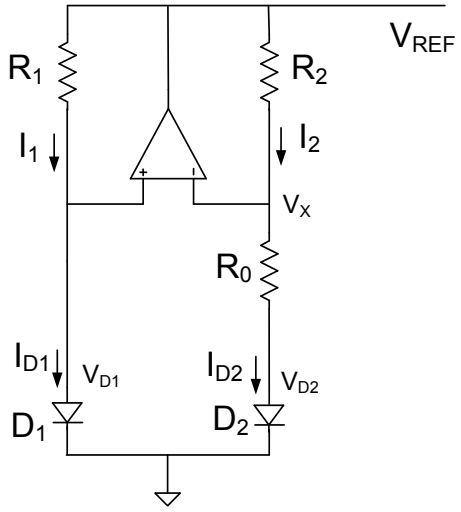


Figure 3 Kuijk bandgap reference circuit

Fig. 4 shows is a modified version of Kuijk bandgap reference circuit with diodes. The circuit of Fig. 3 is similar to that of Fig. 4 but is lacking the MOS transistor. This effectively reduces the open loop gain of the common-mode feedback loop. Note the polarity of the op amp terminals have been reversed because one inversion in the feedback loop associated with the MOS transistor has been removed [2]. The Kuijk bandgap reference circuits require a startup circuit, which is not included to reduce notational complexity. Since the relationship between the output voltage and temperature when a bandgap circuit is operating in the desired operating state is essentially unaffected by the start-up circuit in a well-designed reference circuit, neglecting the startup circuits throughout this thesis will not affect any conclusions that are drawn.

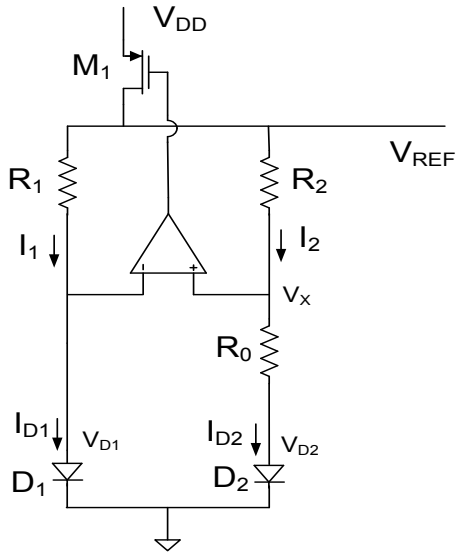


Figure 4 Modified Kuijk bandgap reference circuit with diodes

Though emphasis on this thesis will be on the performance of the Kuijk bandgap reference which was introduced over 40 years ago, this basic structure or a minor variant is still widely used today but more importantly, the key performance properties of most of the bandgap circuits that are used today are similar to those of the Kuijk circuit and the methods of analysis and assessment that will be introduced here can be readily modified to assess the performance of any specific bandgap circuit that is of interest.

2.1 Basic operations of modified Kuijk bandgap reference circuit

The basic operation of a bandgap circuit will be discussed in this section. Consider the modified Kuijk bandgap reference circuit with diode-connected BJTs is shown in Fig. 5. This differs from the circuit of Fig. 4 only in that the diodes have been replaced with diode-connected transistors, which are more readily available than a simple diode in most bulk CMOS processes today. This circuit only has three resistors, one MOS transistors, one op-amp and two temperature sensing bipolar transistors.

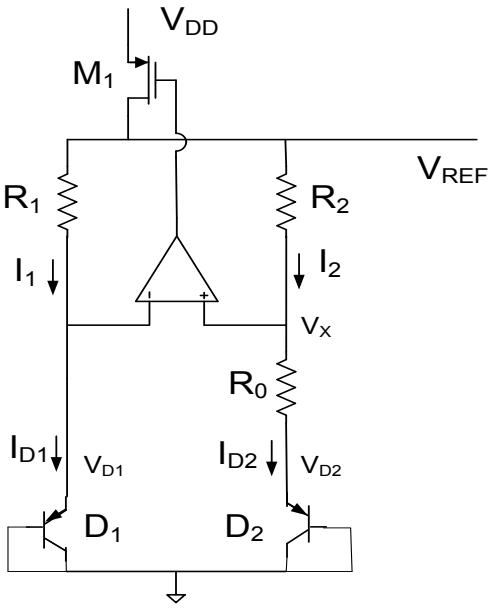


Figure 5 Modified Kuijk bandgap reference circuit with diode-connected BJTs

The high gain operational amplifier forces equal voltages at the non-inverting and inverting input nodes of the amplifier. The voltage reference output is the sum of the emitter-base voltage of D_1 and the voltage drop across R_1. The emitter-base voltage of D_1 provides a negative temperature coefficient voltage. Assuming R_1 and R_2 are same, the high gain operational amplifier ensures an equal voltage drop across R_1 and R_2. The voltage drop across R_0 is equal to the base-emitter voltage difference between D_1 and D_2, which will provide a negative temperature coefficient. Since the current flowing through R_0 and R_2 are the same, the voltage drop across R_2 is a scaled version of the voltage drop across R_0 and the scaling coefficient is the ratio $\frac{R_2}{R_0}$ which is positive. Therefore, if the resistor ratio $\frac{R_2}{R_0}$ is appropriately chosen, the temperature coefficient at the output, V_{REF}, can be forced to vanish at a specific temperature. This temperature is termed the inflection point temperature. The temperature coefficient of V_{REF} will be small in a region around the

inflection point temperature. A mathematical analysis of this bandgap reference is presented in Section 2.2.

The designer has control of the parameter $\frac{R_2}{R_1}$ and $\frac{A_2}{A_1}$. It will be seen in the next section that by changing the ratio of R_2 and R_1 or the ratio $\frac{A_2}{A_1}$, the inflection point can be adjusted to the desired temperature. $\frac{R_2}{R_1}$ can be viewed as the voltage gain of the bandgap reference but should not be confused with the voltage gain of the op amp.

2.2 Standard analysis on modified Kuijk bandgap reference circuit

A qualitative description of the basics operation of the modified Kuijk bandgap reference circuit was given in Section 2.1. A more detailed analysis is presented in this Section. The high gain operational amplifier in this circuit forces equal voltages at the non-inverting and inverting input nodes of the operational amplifier. Assuming the diode-connected transistors can be modeled by the diode Equation. In general BJT can be modeled as (13) ~ (15)

$$I_c = J_S A e^{\frac{V_{BE}}{V_t}} \tag{13}$$

$$I_B = \frac{I_C}{\beta} \tag{14}$$

$$I_E = I_C + I_B \tag{15}$$

J_S is a process parameter that depends on temperature. A is the area factor for the device which is determined by the sizing of the device. V_{BE} is the base-emitter voltage of a

transistor. $V_t = \frac{kT}{q}$ where k is Boltzman's constant, T is the temperature in K, and q is the charge of an electron. β is the current gain of the transistors. From (13), the base-emitter voltage can be expressed as (16),

$$V_{BE} = V_t \ln(I_C) - V_t \ln(J_S A) \tag{16}$$

This BJT model can be applied to the diode-connected transistors in Fig. 5. A_1 and A_2 are the emitter area of transistor D_1 and D_2 in Fig. 5. I_{B1} and I_{C1} are the base and collector currents of transistor D_1 in Fig. 5.

$$I_{D1} = I_{B1} + I_{C1} = (1 + \frac{1}{\beta}) I_{C1} \tag{17}$$

$$V_{D1} = V_t \ln\left(I_{D1}\right) - V_t \ln\left(J_S A_1 \frac{1+\beta}{\beta} \right) \tag{18}$$

Assuming β is infinity then

$$V_{D1} = V_t \ln\left(I_{D1}\right) - V_t \ln\left(J_S A_1\right) \tag{19}$$

Exactly same equations can be applied to transistor D_2

$$V_{D2} = V_t \ln\left(I_{D2}\right) - V_t \ln\left(J_S A_2\right) \tag{20}$$

The operation of the circuit can be described by (21) through (26).

$$V_x = V_{D1} \tag{21}$$

$$I_{D1} = I_1 \quad I_{D2} = I_2 \tag{22}$$

$$V_{REF} = I_2 R_2 + V_{D1} \tag{23}$$

$$I_{D2} = I_2 = \frac{V_{D1} - V_{D2}}{R_0} \tag{24}$$

$$V_{D1} - V_{D2} = V_t \ln\left(\frac{I_{D1}}{I_{D2}}\frac{A_2}{A_1}\right) \tag{25}$$

$$\frac{I_{D1}}{I_{D2}} = \frac{V_{REF} - V_X}{R_1} \Big/ \frac{V_{REF} - V_X}{R_2} = \frac{R_2}{R_1} \tag{26}$$

Therefore (25) can be rewritten as seen in (27) and (28):

$$V_{D1} - V_{D2} = V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right) \tag{27}$$

$$V_{D1} = V_{D2} + V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right) \tag{28}$$

Substitute (20), (24), (25), and (26) into (28) to achieve (29)

$$V_{D1} = V_t \ln\left(\frac{R_2}{R_1}\frac{V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{J_S A_1 R_0}\right) \tag{29}$$

With some tedious manipulations of these equations, the expression of V_{REF} is obtained

$$V_{REF} = \frac{R_2}{R_0} V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right) + V_t \ln\left(\frac{R_2}{R_1}\frac{V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{J_S A_1 R_0}\right) \tag{30}$$

$$J_S = \tilde{J}_{SX}\left[T^m e^{\frac{-V_{G0}}{V_t}}\right] \tag{31}$$

$\tilde{J}_{SX}$ is a geometry independent process parameter, V_{G0} is the silicon bandgap voltage which is about 1.206 V, The parameter m is a temperature-independent constant which is about 2.3. Substituting (31) into (30), V_{REF} can be expressed as (32).

$$V_{REF} = \frac{R_2}{R_0} V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right) + V_t \ln\left(\frac{\frac{R_2}{R_1}\frac{V_t \ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{\tilde{J}_{SX}\left[T^m e^{\frac{-V_{G0}}{V_t}}\right]A_1 R_0}}{}\right) \tag{32}$$

After some manipulation on (32), V_{REF} can be written in the form of (33), where a_1, b_1 and c_1 are shown in (34), (35) and (36)

$$V_{REF} = a_1 + b_1 T + c_1 T \ln T \tag{33}$$

$$a_1 = V_{G0} \tag{34}$$

$$b_1 = \frac{k}{q}\left[\frac{R_2}{R_0}\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right) + \ln\left(\frac{R_2}{R_1}\frac{k}{q}\frac{\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{R_0 A_1 \tilde{J}_{SX}}\right)\right] \tag{35}$$

$$c_1 = \frac{k}{q}(1-m) \tag{36}$$

From (33), the temperature at which the inflection point occurs, T_{INF}, can be found and is given by (57).

$$T_{INF} = e^{-\left(1+\frac{b_1}{c_1}\right)} \tag{37}$$

As well as the output voltage at T_{INF} which is given by (58)

$$V_{REF}(T_{INF}) = a_1 - c_1 T_{INF} \tag{38}$$

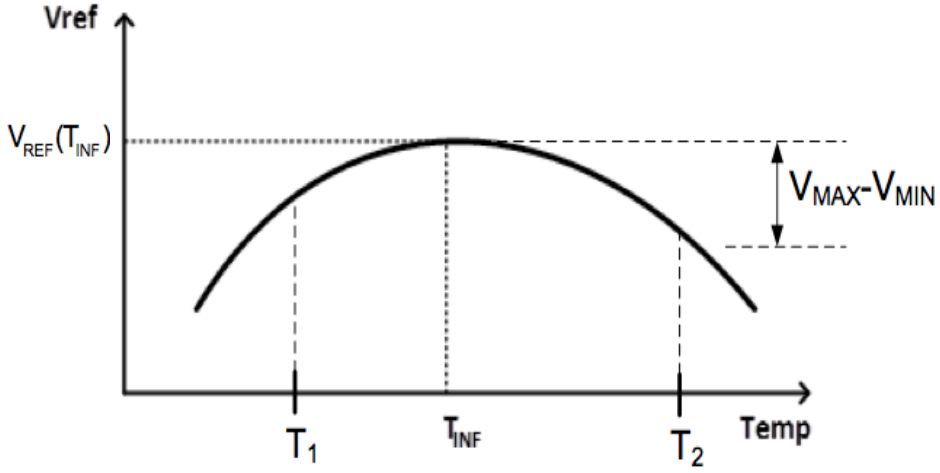


Figure 6 Reference voltage

T_{INF} and $V_{REF}(T_{INF})$ are shown in Fig. 6. The output characteristics of bandgap reference are depicted in Fig. 6. It can be seen that the output of the reference has a single inflection temperature and is concave downward.

From (33), the 1st order and 2nd order temperature coefficient can be found and are expressed in (39) and (40) $V_{REF}(T_{INF})$

$$TC_{1st} = b_1 + c_1(\ln T + 1) \tag{39}$$

$$TC_{2nd} = \frac{c_1}{T} \tag{40}$$

The intended range of operation is the interval [T_1, T2] depicted in Fig. 6. The output at T_1 is depicted as being higher than the output at T_2 in the figure but the circuit could be designed so that the output at T_2 is higher than that at T_1 or, as is often the case, the circuit is often designed so that the outputs at T_1 and T_2 are identical. The total

output deviation over the desired temperature range, V_{MAX}-V_{MIN} is also shown in the figure where in this depiction, $V_{MAX}=V_{REF}(T_{INF})$ and $V_{MIN}=V_{REF}(T_2)$.

The thermal deviations are generally defined in terms of some form of a temperature coefficient (TC). The TC gives an indication of the change in the output voltage of the reference with temperature over a specified temperature range. In this work, the TC is defined by

$$TC = \frac{V_{MAX} - V_{MIN}}{T_2 - T_1} \tag{41}$$

where V_{MAX} and V_{MIN} are the maximum and minimum output voltages over the temperature range $[T_1, T_2]$. The units of the TC are usually $mV/^{\circ}C$ or $\mu V/^{\circ}C$. The definition of the TC in ppm is

$$TC_{ppm} = \frac{V_{MAX} - V_{MIN}}{V_{NOM}(T_2 - T_1)} 10^6 \tag{42}$$

The nominal value, V_{NOM}, is often defined as $V_{NOM}=V_{MAX}$.

The quantities b_1 and c_1 are positive and negative constants respectively which can be viewed as the positive temperature coefficient and the negative temperature coefficient of the bandgap reference. As shown in (35) and (36) , the resistor's temperature variation will affect the positive temperature coefficient but will not affect the negative temperature coefficient provided the same materials are used to make all three resistors.

Note in above analysis, the temperature dependence of resistors and beta of bipolar transistors is not considered. Those non-ideal characteristics will be discussed in Chapter 3.

CHAPTER 3: NONIDEAL CHARACTERISTICS OF KUIJK BANDGAP CIRCUIT

Voltage references are commonly used in power supply regulators, bias generators, references for data converters, and in a host of other applications. In some of these applications the performance requirements are quite relaxed, but in others the performance requirements are very stringent.

Based on the analysis in Chapter 2, a typical V-T curve for the Kuijk bandgap reference circuit shown in Fig. 4 can be obtained. Assuming an ideal diode and that the circuit is designed for an inflection point at 25^{o}C , the results shown in Fig. 7 (blue solid line) is obtained. This curve corresponds to a circuit designed with values given in Table 1.

Table 1 Design Parameters for Kuijk BGR

$R_1(k\Omega)$	$R_2(k\Omega)$	$R_0(k\Omega)$	$A_1 / A_2(\frac{\mu m^2}{\mu m^2})$	$W_1 / L_1(\frac{\mu m}{\mu m})$
10	10	1	1000/9500	3/2

Correspondingly, by using a computer simulator, the two simulated V-T curves for the Kuijk circuit using the diodes and diode connected transistor shown in Fig. 4 and Fig. 5, can be displayed on the same axis as shown in the figure (pink line and red line). In the computer simulation, it was assumed that the temperature coefficient of the resistors was 0 ppm/ ^{o}C and the β of the diode-connected transistors are very large. In simulation β is set to be 100 and $\tilde{J}_{sx}$ is 0.0364 A/um^2.

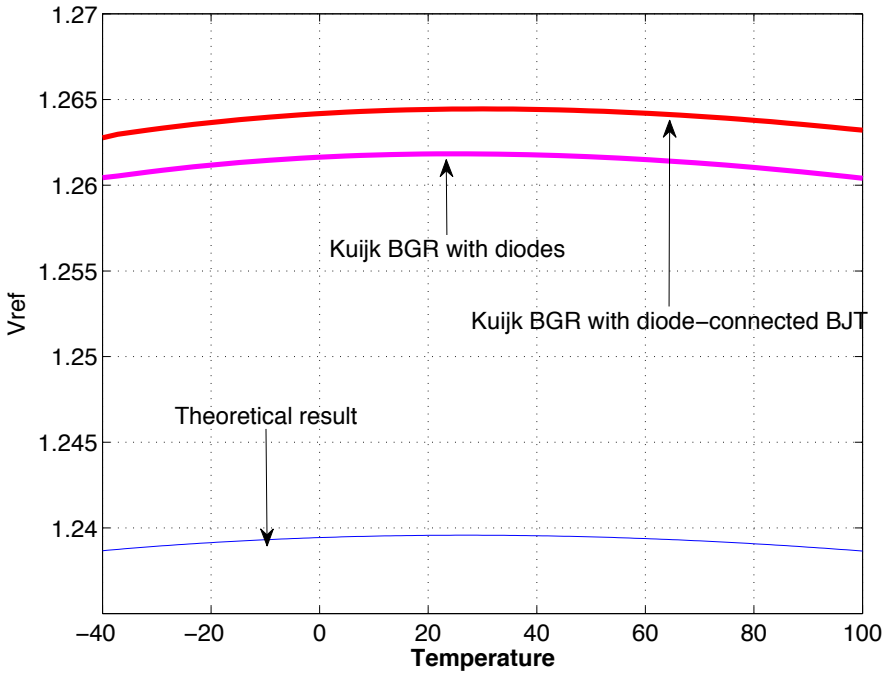


Figure 7 Theory and computer simulation predicts

It can be observed from Fig. 7 that the predicted reference voltage is around 1.24 V at 25°C based upon the simple theoretical models and the TC is about 5 ppm/°C. From computer simulations, the predicted reference voltage is about 1.2618 V with a diode at 30°C. The TC is about 8.5 ppm/°C. The reference voltage with a diode-connected transistor is around 1.2645 V at 30°C. The TC is about 9.6 ppm/°C. It can be observed that there is a small difference between the simulated results and the analytical results. This difference is due to small model errors in the rather simple analytical formulation. The level shift between the analytical formulation and the computer simulations does not cause a problem in most applications.

In this chapter, the non-ideal effects of the diode-connected BJT and the temperature dependence of the resistors will be considered. The analysis in Chapter 2 did not include the temperature dependence of resistors, base-spreading resistance of the

diode-connected transistors, resistance in the layout of the transistors, or the temperature dependence of the forward current gain beta of the bipolar transistors. However, these non-ideal characteristics are representative of model errors that can impact the output of bandgap voltage references. Furthermore, the non-ideal characteristics contribute to discrepancies between analytical, simulated, and experimental values for the inflection point and temperature coefficients. In this chapter, these non-ideal effects will be included in the analytical characterization of the modified Kuijk bandgap reference circuit. Simulation results including these effects can be found in Chapter 4.

3.1 Bipolar transistors in CMOS technology

In a standard bulk CMOS process there are few options for constructing bipolar transistors. There is a lateral n-well to p-sub to n-well (npn) transistor available. Also there is a lateral n-diff to p-sub to n-diff device. But conventional wisdom suggests that in an N-well CMOS process, the substrate PNP bipolar transistor [21] is best suited for constructing the diode-connected transistor needed in bandgap references. This transistor consists of P-type source/drain implant for the emitter, N-well for the base, and the P-substrate for the collector.

Conventionally, the bipolar junction transistor is designed such that the doping concentration of its emitter is higher than the doping concentration of the base and with a base doping concentration that is higher than that of the collector. More importantly, the base region is very thin. With this approach, close to 100% of the injected carriers from the emitter pass through the thin base region without recombination in the base region. These injected carriers are collected by collector and become contributors to the collector

current. A low doping concentration of the collector is necessary to achieve a large reverse breakdown voltage of the device. In the substrate PNP transistor, the N-well is used to form its base region. Modern CMOS processes usually have channel lengths that are much shorter than one micron. Due to the short channel effect, the doping profile needs to be higher in order to prevent punch-through of short channels. The heavier well doping increases the Gummel number of the substrate PNP and therefore reduces its gain [21]. The base region under the p+ emitter is also quite thick and thus further reducing the current gain.

3.2 Macro-model for base spreading resistance of bipolar transistor

A bipolar transistor with a large emitter area has a considerable parasitic resistance in its base region. This resistance in the base region is termed the base spreading resistance. The base spreading resistance is distinct from the series base resistance, which represents the resistance in the base diffusion from the physical base terminal to the actual base of the transistor. The base spreading resistance causes current crowding in the base region due to the variation in the effective base-emitter voltage throughout the base region. These effects become worse when the base region is thick and the resistivity is high. This occurs when the n-well is used to form the base region in the substrate PNP transistor that is available in bulk CMOS processes. For typical layouts, the current density in the base region is higher in the vicinity of the base contacts. Due to the distributed nature of the exponential dependence of collector current on base-emitter voltage, an explicit analytical expression for V_{REF} that includes base spreading resistance effects cannot be obtained.

A cross-sectional view of a substrate PNP bipolar transistor is shown in Fig. 8 where base contacts are made to both the left side and the right side of the base region. This transistor consists of a P-type source/drain implant for the emitter, an N-well for the base, and the P-substrate for the collector. R_B is the series base resistance of the bipolar transistor and drawn vertically in the figure. The base spreading resistance is the distributed resistor drawn horizontally in the base region of the transistor and denoted as BSR.

In order to model the distributed base spreading resistance, the base region is sliced vertically into several pieces. Each slice comprises of a bipolar transistor with a series base resistance. These individual slices can be connected in parallel to obtain the lumped model shown in Fig. 9. When one increases the number of slices the model becomes more accurate, but increasingly more complicated. In most applications, little improvement is obtained after the number of slices goes beyond 8 in a simple layout of the device. In this work, the effects of base spreading resistance will be investigated using 2-piece, 4-piece and 8-piece models.

A macro-model if the bipolar transistor using a 4-piece base spreading resistance model and a single base contact on the left side is shown in Fig. 10. The resistors of value R in this model are used to model the base spreading resistance. The value of these resistors depends upon the geometry of the base region and both the thickness and doping density of the base region. In this model, the base spreading resistance will cause the base-emitter voltages in the four bipolar transistors to be different with a voltage drop in the base-emitter voltage successively occurring in the four bipolar transistors when moving from left to right in the figure. This drop in base-emitter voltages will induce a

corresponding drop in the collector currents and hence a non-uniform current density in the emitter region. The higher current density on the left side of the emitter region than in the middle or right side of the region gives rise to a phenomenon termed “current crowding”. Where current crowding occurs in a transistor depends both upon the layout of the transistor and the number and location of the contacts to the base region. Although not shown in Fig. 10, if a base contact were made on both the left side and the right side of the transistor, current crowding would occur on both the left side and the right side of the transistor.

There are many different ways to layout the substrate PNP bipolar transistor and the layout impacts both the series base resistance and the base spreading resistance. The research only considers the layout for the substrate PNP bipolar transistor shown in Fig. 11 which has a series of base contacts on the left side of the base region. Fig. 11 is a featured layout, which means the width and the length of the emitter are fixed. The only way to change the emitter size is by adjusting the multiplier.

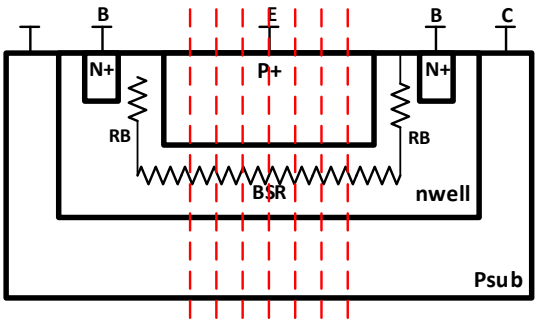


Figure 8 Cross-section view of a PNP bipolar transistor

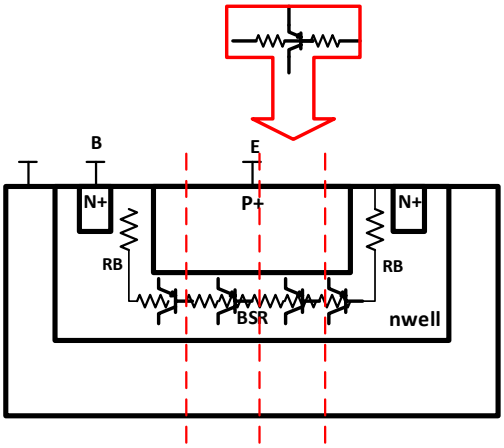


Figure 9 Substrate PNP bipolar transistor with sliced base region

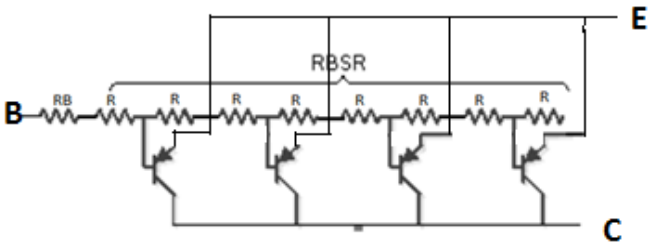


Figure 10 A 4-piece base spreading resistance model

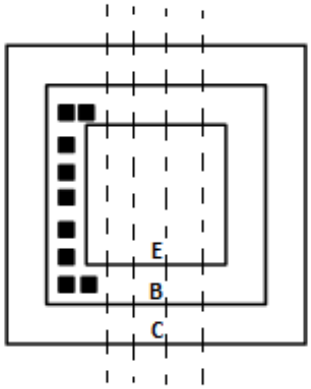


Figure 11 Layout of PNP bipolar transistor

The 2-piece and 8-piece macro-models can be developed by modifying the circuit of Fig. 10 by changing the number of paralleled bipolar transistors and the corresponding value of the base spreading resistors. In the macro-model, it has been assumed that the square emitter layout of Fig. 11 was used for the Emitter and Base regions of the BJT.

Each of the resistors in the macro-model are given by (44_a) where m is the number of segments in the model and R_{SH} is the emitter-pinched sheet resistance of the n-well.

$$R = \frac{R_{SH}}{2m} \tag{43_a}$$

Fig. 10 is a macro-model for the featured layout as shown in Fig. 11. The sliced base spreading resistance within the featured layout is modeled by (43_a). By adjusting the multipliers, one can decide the number of the featured layouts connecting in parallel. Considering the multiplier M, the base spreading resistors are given by (43_b).

$$R = \frac{R_{SH}}{2m * M} \tag{43_b}$$

3.3 Effects of temperature dependent beta on voltage reference

In this section, the temperature dependence of beta will be addressed. (30) was developed using a standard diode model for the diode-connected BJT so does not include the temperature dependence of the transistors' β. A modification of the results to include the effects of β is straightforward. The model of temperature dependence of β, is shown in (44), where XTB is a constant. T_1 is any reference temperature.

$$\beta(T) = \beta(T_1)(\frac{T}{T_1})^{XTB} \tag{45}$$

The characteristics of the BJT can be modeled by (45) to (47). V_{BE} is the base-emitter voltage, which is labeled as V_{D1} in Fig. 5. A_1 is the emitter area of transistor, D_1 as labeled in Fig. 5.

$$I_{D1} = I_{E1} = I_{C1} + I_{B1} \tag{46}$$

$$I_{C1} = \beta(T) I_{B1} \tag{47}$$

$$I_{E1} = (1 + \frac{1}{\beta(T)}) J_s A_1 e^{\frac{V_{BE}}{V_t}} \tag{48}$$

It follows from (21)-(29) that the voltage V_{D1} can be expressed as

$$V_{D1} = V_t \ln(I_{D1}) - V_t \ln(J_s A_1 \frac{\beta(T)+1}{\beta(T)}) \tag{49}$$

Substituting from (45) into (49) the expression for V_{D1} becomes

$$V_{D1} = V_t \ln(\frac{R_2}{R_1} \frac{V_t \ln(\frac{R_2}{R_1}\frac{A_2}{A_1})}{R_0 J_s A_1} \frac{\beta(T_1)(\frac{T}{T_1})^{XTB}}{1+\beta(T_1)(\frac{T}{T_1})^{XTB}}) \tag{50}$$

The effects of the temperature-dependent beta can now be obtained following the approach of Section 2.2. The only difference the temperature dependent beta causes is that (30) changes to (50)

$$V_{ref} = \frac{R_2}{R_0} V_t \ln(\frac{R_2}{R_1}\frac{A_2}{A_1}) + V_t \ln(\frac{R_2}{R_1} \frac{V_t \ln(\frac{R_2}{R_1}\frac{A_2}{A_1})}{R_0 J_s A_1} \frac{\beta(T_1)(\frac{T}{T_1})^{XTB}}{1+\beta(T_1)(\frac{T}{T_1})^{XTB}}) \tag{51}$$

Following the same manipulations that were used in Section 2.2 it follows that V_{REF} can be expressed in the form of (51)

$$V_{ref} = a_2 + b_2 T + c_2 T \ln T \tag{52}$$

where

$$a_2 = V_{G0} \tag{53}$$

$$b_2 = [\frac{R_2}{R_0}\ln(\frac{R_2}{R_1}\frac{A_2}{A_1}) + \ln(\frac{R_2\beta(T_1)\frac{k}{q}\ln(\frac{R_2}{R_1}\frac{A_2}{A_1})}{R_1R_0A_{D1}\widetilde{J_{sx}}}) - [XTB\ln(\frac{\beta(T_1)}{T_1}) + \ln(\beta(T_1))]]\frac{k}{q} \tag{54}$$

$$c_2 = (1 - m - XTB)\frac{k}{q} \tag{55}$$

From (52), the 1st order and 2nd order temperature coefficient can be found in (55) and (56)

$$TC_{1st} = b_2 + c_2(\ln T + 1) \tag{56}$$

$$TC_{2nd} = \frac{c_2}{T} \tag{57}$$

Likewise, the inflection point temperature and the output at the inflection temperature have the same form as (37) and (38) and can be expressed as

$$T_{INF} = e^{-\left(1+\frac{b_2}{c_2}\right)} \tag{58}$$

$$V_{REF}(T_{INF}) = a_2 - c_2 T_{INF} \tag{59}$$

T_{INF} and $V_0(T_{INF})$ are shown in Fig. 6. Since c_2 in (55) remains unchanged, b_2 in (54) increases, it follows that the positive temperature coefficient will be increased by including the temperature dependence of β. However, the negative temperature coefficient stays the same. As a result, the inflection point will be shifted to a higher temperature. Simulation results are shown in Chapter 4.

3.4 Effects of temperature dependent resistors on voltage reference

In a CMOS process, the resistance of integrated resistors will change with temperature. The temperature coefficient is widely used to characterize the temperature characteristics of a resistor and it is often expressed in units of ppm/°C. The temperature coefficient of n-well resistors can vary from 2000 ppm/°C to 7500 ppm/°C from one process to another [6],[21]. Process variations can lead to deviations in the absolute value of resistors by as much as +/-20%. This directly affects the inflection point of the voltage reference output and the PTAT currents.

In this thesis, it will be assumed that the temperature coefficient of the resistors used in the bandgap circuit of Kuijk are constant. With this assumption, the model of a temperature dependent resistor is given in (60), where R_0 is the value of a resistor specified at a nominal temperature T_0 and T is the actual temperature of the resistor. The parameter TCR is the temperature coefficient of the resistor.

With this model, the solution of (33) can be modified to obtain V_{REF} when the resistors are temperature dependent. This modification only requires a change in b_1 of (35) as shown in (60). The quantities a_1 and c_1 stay the same.

$$R(T) = R_0\left[1 + TCR \bullet (T - T_0)\right] \tag{59}$$

$$b_1 = \frac{k}{q}\left[\frac{R_2 + R_2 TCR(T - T_0)}{R_0 + R_0 TCR(T - T_0)} \ln\left(\frac{R_2 + R_2 TCR(T - T_0)}{R_1 + R_1 TCR(T - T_0)} \frac{A_2}{A_1}\right) + \ln\left(\frac{R_2 + R_2 TCR(T - T_0)}{R_1 + R_1 TCR(T - T_0)} \frac{k}{q} \frac{\ln\left(\frac{R_2 + R_2 TCR(T - T_0)}{R_1 + R_1 TCR(T - T_0)} \frac{A_2}{A_1}\right)}{[R_0 + R_0 TCR(T - T_0)] A_1 \tilde{J}_{SX}}\right)\right] \tag{60}$$

The same resistor types are invariably used to realize the three resistors. With this standard assumption, the TCR does not affect resistor ratios in the expression for b_1 and thus (60) can be expressed as

$$b_1 = \frac{k}{q}\left[\frac{R_2}{R_0}\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)+\ln\left(\frac{R_2}{R_1}\frac{k}{q}\frac{\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{R_0(T_0)A_1\tilde{J}_{SX}}\right)-\ln\left(1+[T-T_0]TCR\right)\right] \tag{61}$$

Since the TCR is relatively small, a truncated Taylor's series can be used to approximate the last term resulting in the expression

$$b_1 \simeq \frac{k}{q}\left[\frac{R_2}{R_0}\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)+\ln\left(\frac{R_2}{R_1}\frac{k}{q}\frac{\ln\left(\frac{R_2}{R_1}\frac{A_2}{A_1}\right)}{R_0(T_0)A_1\tilde{J}_{SX}}\right)-[T-T_0]TCR\right] \tag{62}$$

The temperature coefficient of resistors has an impact on b_1 and introduces a small second-order dependence on T. On the other hand, the temperature coefficient of the resistors do not have any impact on the negative temperature coefficient term, c_1, or the constant term a_1 in (33). Though the inflection point expression will change somewhat since the second-order temperature coefficient will change the functional form of (33), an approximation of the inflection point is shown in (37). It can be observed from (37) that the temperature dependence of the resistors will cause a shift in the inflection point due to changes in b_1 and $V_{REF}(T_{INF})$ will also be shifted.

The base spreading resistance of the bipolar transistor will also experience variations due to temperature changes. An explicit analytical expression for V_{REF} that includes the base spreading resistance effects cannot be obtained for the Kuijk reference.

The temperature coefficient of that base spreading resistance is likely different that of the three resistors in the Kuijk bandgap reference circuit shown in Fig. 5 since the pinched n-well region will likely serve as the base of the BJT whereas different processing steps (e.g. polysilicon) will likely be used to implement the resistors. But it is not the difference in the processing steps and corresponding temperature coefficients but rather the highly nonlinearity of the circuit that prevents the derivation of explicit analytical expressions for the effects of the base spreading resistance. The impact of the temperature dependent base spreading resistance will be observed by simulation. The simulated results will be shown in Chapter 4.

CHAPTER 4: SIMULATION RESULTS

In previous chapters, it shows the effects of non-ideal characteristics of Kuijk bandgap reference circuit on the voltage reference output. Simulation results will be included in this chapter.

In this chapter, we will first investigate the non-ideal resistance, base spreading resistance, and transistor β effects separately and then look at the combined effects. The simulated results for the individual effects are shown in Section 4.2, Section 4.3 and Section 4.4. The combined effects on the voltage reference output are considered in Section 4.5.

Seven tasks have been established for the purpose of exploring the effects of the non-ideal characteristics of bipolar transistor on the voltage reference output. A summary of these tasks is shown in Table 2.

Table 2 Tasks exploring the non-ideal characteristics of the BGR; X: Temperature dependent, O: Temperature independent

Task No.	β	R_0, R_1, R_2,	R_{BSR} (1.1K)	R_B
1	O	O	O	O
2	O	X	O	O
3	O	O	X	O
4	O	O	O	X
6	X	O	O	O
7	X	X	X	X

In this table, β is the forward current gain of the PNP bipolar transistor. R_0, R_1 and R_2 are the three resistors as labeled in Fig. 5. R_{BSR} is the effective base spreading resistance in a vertical substrate PNP bipolar transistor, and R_B is the series base

resistance. Task 1 can be considered as a reference where all the components are ideal and temperature independent. Comparisons between Task 1 and each one of the other six tasks will be shown in the following sections.

Nonlinearity and offset voltage of the operational amplifier will also have effects on the voltage reference output and these issues have been considered by others [7]-[11], [22], [24]. Effects due to the operational amplifier will not be considered in this thesis. In this thesis, an ideal voltage controlled voltage source (VCVS) with a very high gain is used to model the operational amplifier.

4.1 Voltage reference without non-ideal characteristics of BJT

In Chapter 2, the standard analysis of Kuijk bandgap reference circuit has been presented. In a 0.18μm CMOS process, the Kuijk bandgap reference circuit has been simulated. The simulation environment is shown in Table 3. V_{REF} is shown in Fig. 12.

Table 3 Simulation Environment for the ideal case

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	0	10	0	1	0

Design Parameters in 0.18μm CMOS Process						
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β
36	0	0	NO	0	0	100

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{1000}{9500}$	$\frac{3}{2}$

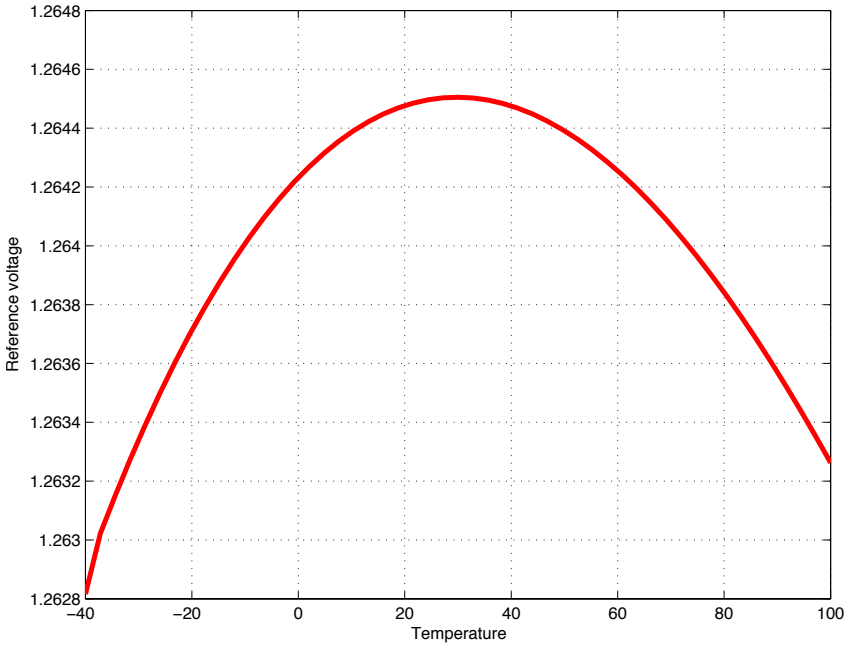


Figure 12 Reference voltages in ideal case

As it is shown in Fig. 12, the reference voltage equals to 1.2645V at 30°C and the TC is about 9.6 ppm/°C. This is an expanded view of the same simulation results that were included in Fig. 7 of the previous chapter.

4.2 Effects of base spreading resistance of bipolar transistor

In Section 3.2, it was illustrated that the parasitic base spreading resistance of a PNP bipolar transistor in modern CMOS technology can be large and it was stated that this large base spreading resistance would cause a variation in the voltage reference output. In this section, the effects of base spreading resistance on the voltage reference output will be quantified.

Initially consider diode connected BJTs with a square emitter region of area 1000 μm^2 and a pinched n-well sheet resistance of R_{SH}=1500 ohms/square. Simulation results including the effects of the base-spreading resistance are shown in Fig. 13. From the

simulation results, it can be observed that with this layout, the base spreading resistance causes an upward shift in the output voltage of about 6mV but little change in either the inflection point or the temperature coefficient. The 8-piece base spreading resistance macro model is more accurate than the 2-piece base spreading resistance macro model. As the number of segments in the model increases, the simulated results for the voltage reference output become more accurate. However, from the simulation results, it can be observed that further increases in the number of the segments in the macro model beyond 8 slices will only marginally improve the accuracy of the voltage reference output. Therefore, an 8-piece base spreading resistance macro model has been used in the simulations. The simulation environment is shown in Table 4.

Table 4 Simulation Environments for BSR

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	0	10	0	1	0

Design Parameters in 0.18μm CMOS Process						
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β
36	0	1.5	2,4,8-Piece	0	0	100

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{1000}{9500}$	$\frac{3}{2}$

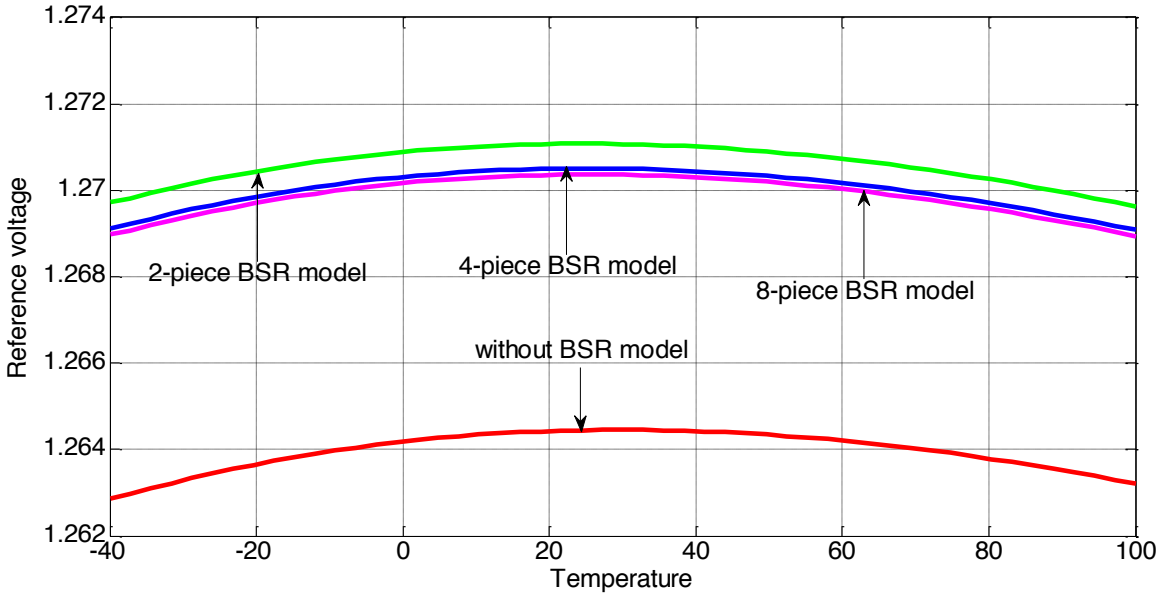


Figure 13 Effects of base spreading resistance on voltage reference output

The temperature dependence of the base spreading resistance is also of concern. Assuming the temperature coefficient of the pinched n-well resistor is 1500 ppm/°C [25], the simulated output of the reference shown in Fig. 14 is obtained. Relative to the output with a temperature-independent base spreading resistance model, the inflection point barely moves and the voltage reference output increases by about 5 mV. The temperature dependence of the base spreading resistance causes little change in the TC of the voltage reference output with this process and the layout shown in Fig. 11.

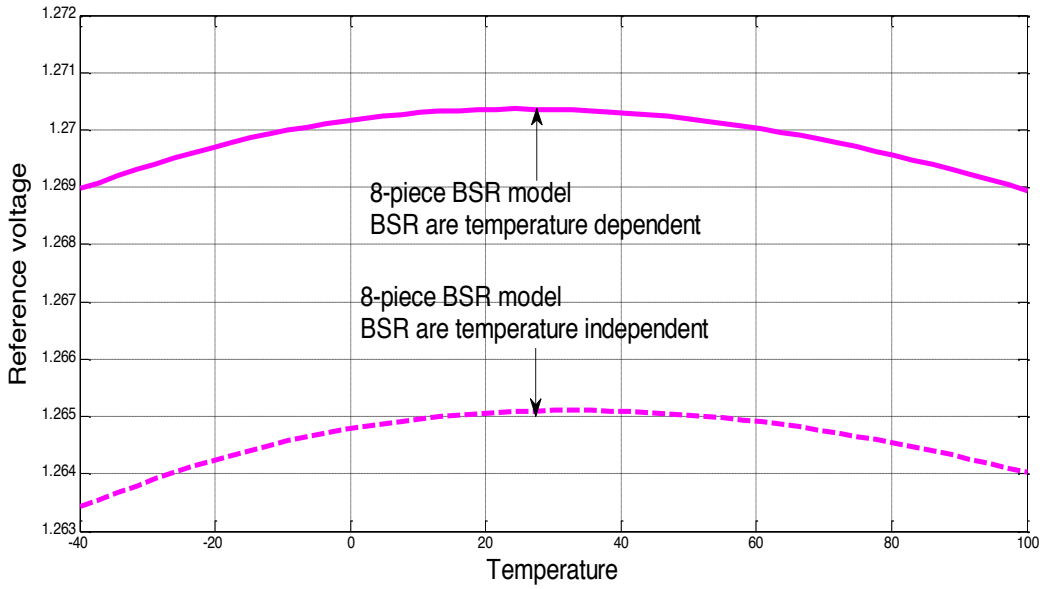


Figure 14 Effects of temperature dependent base spreading resistance on V_{REF}

4.3 Effects of temperature dependent beta on voltage reference output

The analysis on the temperature dependence of β has been discussed in Section 3.3. The temperature dependence of β is shown in (44). In the simulations, T_1 is set to 300K. A plot of β versus temperature for both the ideal case and the temperature dependent case are given in Fig. 15.

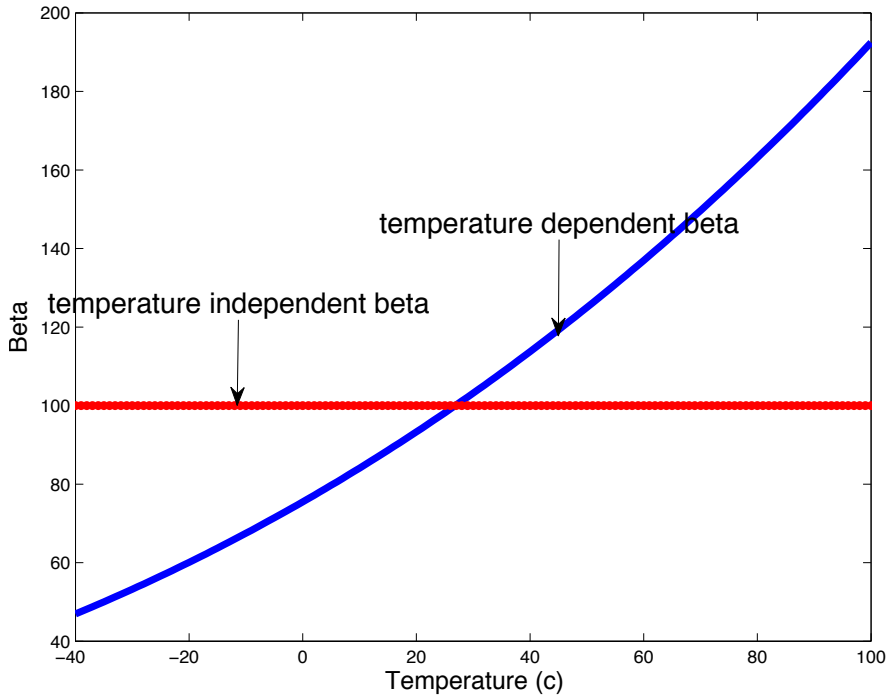


Figure 15 β versus temperature

As shown in (54) and (55), that by including the temperature dependence of β, the positive temperature coefficient will be increased. However, the negative TC stays about the same. As a result, the inflection point will be shifted to a higher temperature. Simulation results are shown as Fig. 16. The temperature dependence of β causes the inflection point of the voltage reference output to move from 30 °C to about 75 °C, which is an increase by 45 °C. Without calibration, the TC is increased from 9.6 ppm/°C to 36.1 ppm/°C which is around 3.8 times incensement. With a two-point calibration to center the inflection point at 30°C, the TC is increased to 26.4 ppm/°C which is around a 2.8 times incensement. From these simulation results, it is apparent that the temperature dependence of β can have a strong effect on the voltage reference in at least some semiconductor processes. The simulation environment is shown in Table 5.

Table 5 Simulation environment for temperature dependent β

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	0	10	0	1	0

Design Parameters in 0.18μm CMOS Process							
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β_0	$T_1(K)$
36	0	0	NO	0	1.5	100	300

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{1000}{9500}$	$\frac{3}{2}$

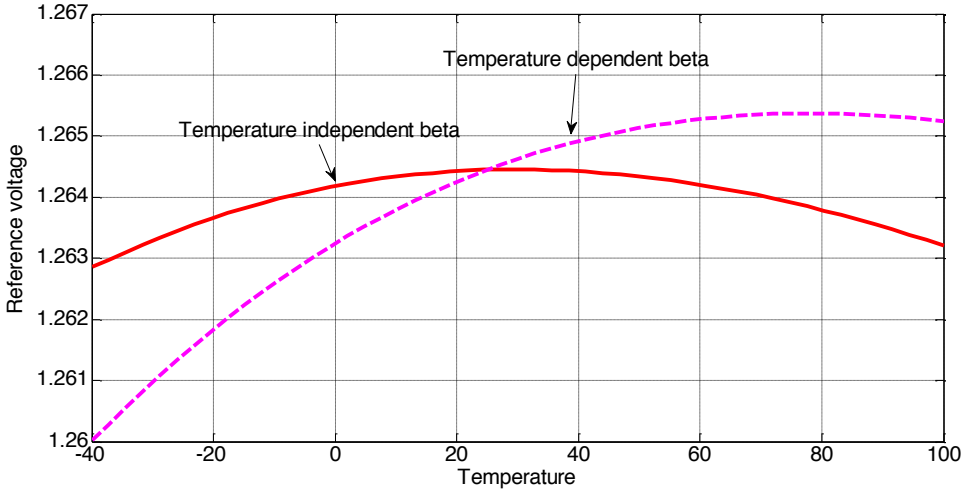


Figure 16 Effects of temperature dependent beta on voltage reference output

4.4 Effects of temperature dependent resistors on voltage reference output

In Task 2, the temperature dependence of resistors R_0, R_1 and R_2 on the voltage reference output will be explored. Only R_0, R_1 and R_2 are temperature dependent resistors. Base resistors (R_B) and base spreading resistors are temperature independent. The temperature coefficients of R_0, R_1 and R_2 are 6000 ppm/°C [6]. This simulation does not include the base spreading resistance in the bipolar transistors. Simulation results are shown as Fig. 17. The simulation results suggest that the TCR of R_0, R_1 and R_2 will move the inflection point to a lower temperature by about 7 °C and the voltage reference output will shift up by about 23 mV. Without calibration, the TC will increase by about 1.8 times. The simulation environment is shown in Table 6.

Table 6 Simulation environment for temperature dependent resistors

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	6000	10	6000	1	6000

Design Parameters in 0.18μm CMOS Process					
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB
36	0	0	NO	0	0

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{1000}{9500}$	$\frac{3}{2}$

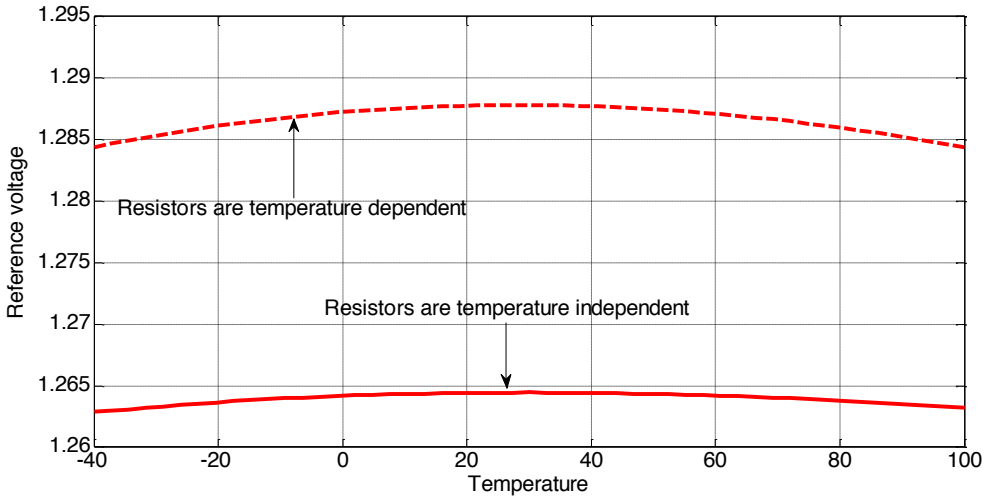


Figure 17 Comparison between Task1 and ask2 without BSR model

The temperature dependence of base resistance R_B will also affect the voltage reference output. The simulation environment is shown in Table 7.

Table 7 Simulation environment for temperature dependent R_B

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	0	10	0	1	0

Design Parameters in 0.18μm CMOS Process					
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB
36	3000	0	NO	0	0

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{1000}{9500}$	$\frac{3}{2}$

As shown in Fig. 18, due to the temperature dependence of R_B, the inflection point changes from 30°C to 33°C and the temperature coefficient barely changed. This small change in the output may be dominantly attributable to the observation that the value of R_B is very small. Other layouts that might have a significantly larger value of R_B may be significantly impacted by the temperature dependence of R_B.

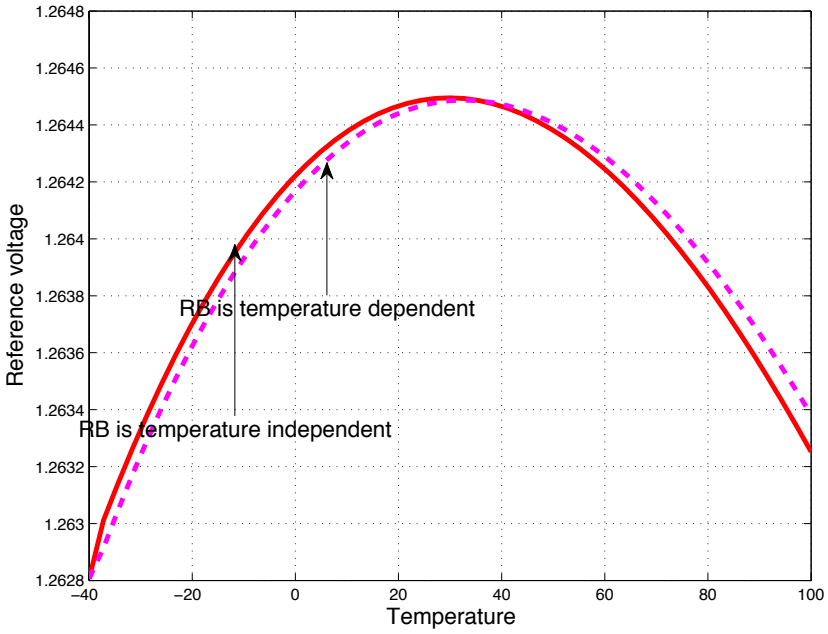


Figure 18 Effects of temperature dependent R_B on voltage reference output

4.5 Overall effects on voltage reference output due to non-ideal characteristics of kuijk bandgap reference circuit

The effects of base spreading resistance of a BJT, the temperature dependence of β and the temperature dependence of resistors are shown through Section 4.2 to 4.4. A summary of the contribution to the output shifts in inflection point, inflection point magnitude, and TC due to each of the effects is shown in Table 7.

Table 8 Summary of each non-ideal characteristics effect on reference voltage

	Inflection point	Inflection point magnitude	TC
Ideal case	30°C	1.2645 V	9.6 ppm/°C
Effects of applying 8-piece BSR model	30°C	1.2705 V	9.6 ppm/°C
Effects of temp dependent β	75°C	1.2654 V	36.1 ppm/°C
Effects of temp dependent R_0,R_1,R_2	23°C	1.2875 V	17.7 ppm/°C
Effects of temp dependent R_B	33°C	1.2645 V	9.6 ppm/°C
Effects of temp dependent R_{BSR}	22°C	1.2695 V	10 ppm/°C
Overall effects including BSR, temp dependent resistors and β.	55°C	1.2793V	37.41ppm/°C

In Task 7, all of the non-ideal characteristics of the bipolar transistor and the resistors are considered together. The simulation environment is shown in Table 9. The simulation results are shown in Fig. 19.

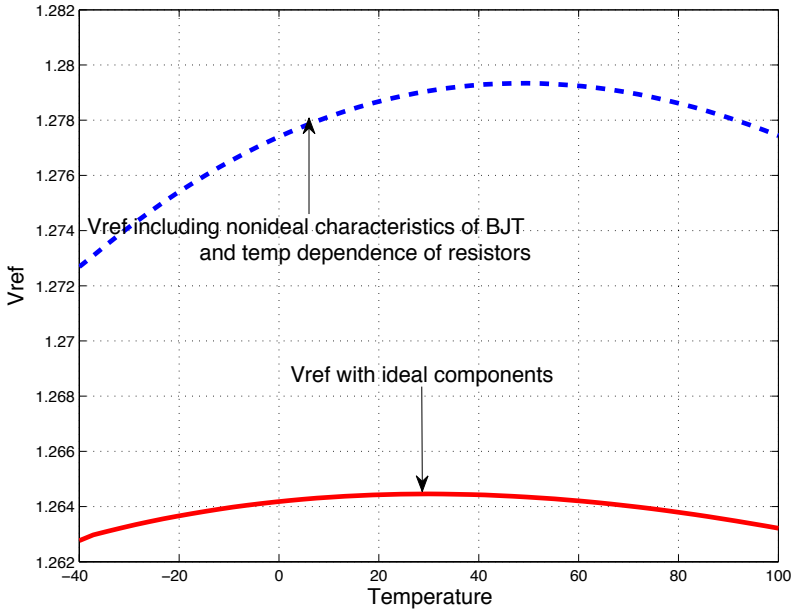


Figure 19 Overall non-ideal characteristics of bipolar transistor on V_{REF}

Table 9 Simulation environment including non-ideal characteristics

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
10	6000	10	6000	1	6000

Design Parameters in 0.18μm CMOS Process							
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β_0	$T_1(K)$
36	3000	1.5	8piece	3000	1.5	100	300

Design Parameters in 0.18μm CMOS Process		
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$	R (Ω)
$\frac{1000}{9500}$	$\frac{3}{2}$	10

The simulation result suggests that the inflection point moves to a higher temperature by 25 °C and the voltage reference output will shift up by 14.8 mV. Without calibration, the TC will increase from 9.6 ppm/°C to 37.41 ppm/°C, which is about a 3.9 times increase. These results are listed at the last row in Table 7 and show how the combined effects compare with the individual contributors to performance degradation in the bandgap reference.

Overall, the temperature dependence of β dominantly shifts the inflection point to a higher temperature and on the other hand, the temperature dependence of R_0, R_1, R_2 and R_{BSR} move the inflection point to a lower temperature. When combine them together, the inflection point increases by about 25°C. The effects of the temperature dependent R_0, R_1,

R_2 mainly affect the magnitude of the inflection point. Temperature coefficient of the reference output voltage can be greatly affected by the temperature dependent β and R_0, R_1, R_2.

4.6 Simulated reference output voltage with a realistic size

In the previous sections, the emitter sizes for transistors D_1 and D_2 shown in Fig. 5 are $1000\mu m^2$ and $9500\mu m^2$. Assuming the pinched n-well sheet resistance is 1.5 kΩ/□, each sliced piece of the base spreading resistance R is 10 Ω. In a more realistic simulation, set the emitter sizes for D_1 and D_2 to be $100\mu m^2$ and $950\mu m^2$. With the smaller emitter sizes, each sliced piece of the base spreading resistance R will be increased to 100Ω. Fig. 20 compares the simulated reference output voltage between a realistic emitter size and a large emitter size. Table 9 is the simulation environment.

Table 10 Simulation environment for realistic emitter area

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
9.85	0	9.85	0	1.05	0

Design Parameters in 0.18μm CMOS Process						
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β
36	0	0	NO	0	0	100

Design Parameters in 0.18μm CMOS Process	
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$
$\frac{200}{800}$	$\frac{3}{2}$

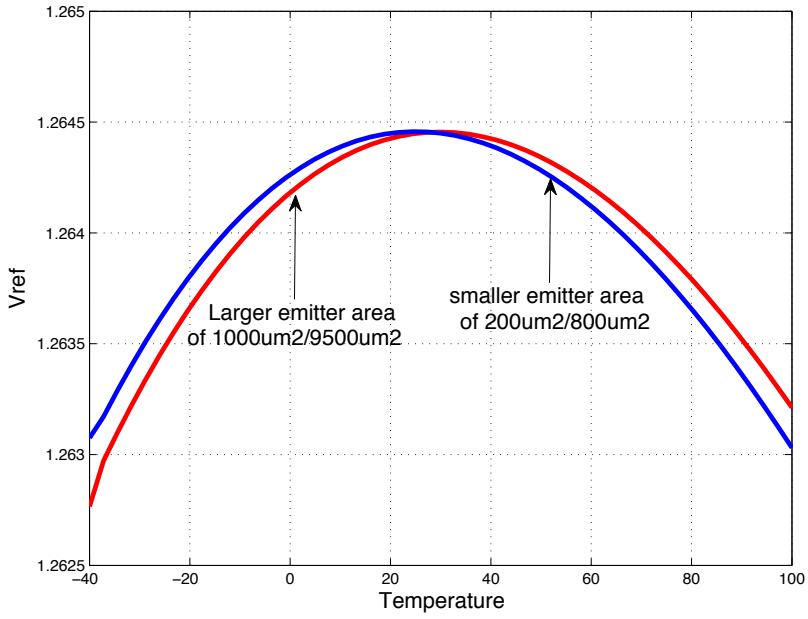


Figure 20 Simulated V_{REF} with a realistic emitter size

As shown in Fig. 20 that, with a realistic emitter size the inflection point has been adjusted to 30 °C. The TC has changed from 9.6ppm/ ° C to 8.7ppm/ ° C.

By considering the effects of base spreading resistance, an 8-piece BSR model has been applied to the Kuijk bandgap reference circuit. The simulation environment is shown as Table 11.

Table 11 Simulation environment for realistic emitter area with 8-piece BSR model

Design Parameters in 0.18μm CMOS Process					
$R_1(k\Omega)$	$TCR_1(ppm/°C)$	$R_2(k\Omega)$	$TCR_2(ppm/°C)$	$R_0(k\Omega)$	$TCR_0(ppm/°C)$
9.85	0	9.85	0	1.05	0

Design Parameters in 0.18μm CMOS Process						
$R_B(\Omega)$	$TCR_B(ppm/°C)$	$R_{SH}(k\Omega)$	BSR model	$TCR_{BSR}(ppm/°C)$	XTB	β
36	0	1.5	8-piece	0	0	100

Design Parameters in 0.18μm CMOS Process		
$\frac{A_{E1}}{A_{E2}}$ $(\frac{\mu m^2}{\mu m^2})$	$\frac{W_1}{L_1}$ $(\frac{\mu m}{\mu m})$	R (Ω)
$\frac{200}{800}$	$\frac{3}{2}$	50

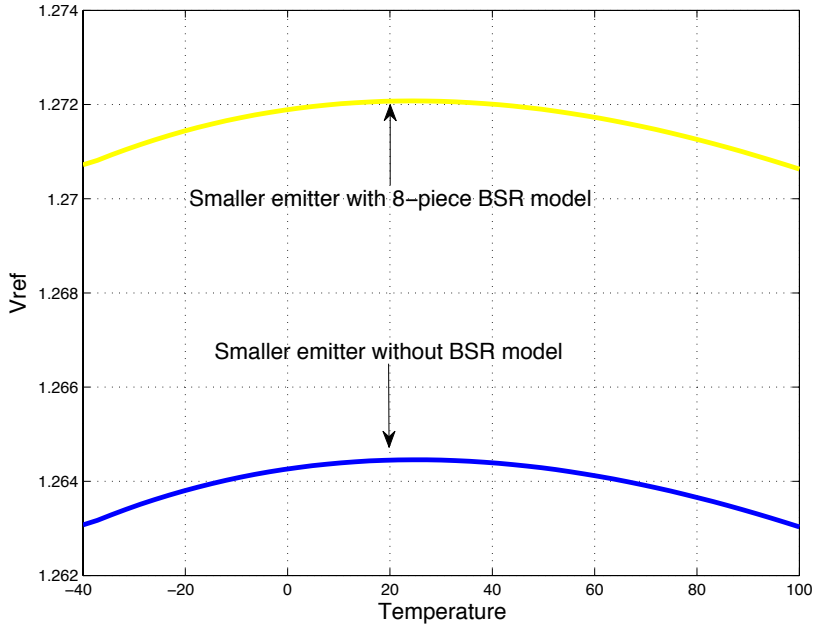


Figure 21 Simulated V_{REF} with a smaller emitter area and 8-piece BSR model

The simulation result is shown in Fig. 21. By applying the 8-piece BSR model to the smaller emitter area BJT, at the inflection point, V_{REF} is increased from 1.2644 V to 1.2721 V. Inflection point is still at 30 ° C and TC has barely changed.

In modern technologies, the feature layout of a BJT is fixed. Multipliers are used to adjust the total emitter area of BJT by putting featured devices into parallel. The smaller the emitter area will increase each sliced base spreading resistance. Therefore, smaller devices will suffer a more significant base spreading resistance effects on the reference output voltage.

CHAPTER 5: CALIBRATION ON VOLTAGE REFERENCE OUTPUT

Precision bandgap references are a critical component in many analog and mixed-signal integrated circuits. The thermal stability of the voltage reference output is very important in the performance of many systems. As the industry moves to system-on-a-chip scale circuits where the supply voltage drops dramatically, the performance requirements on the voltage reference output are becoming more stringent. Although bandgap circuits are designed to provide a low temperature sensitivity, invariably process variations cause a significant shift in the inflection point and correspondingly a considerable increase in temperature dependence. Process variations can cause the inflection point to shift to higher or to lower temperatures. This shift in inflection point and the corresponding degradation in temperature insensitivity is unacceptably large in many applications. Calibration is an effective method for achieving high accuracy and acceptable temperature insensitivity and most bandgap circuits are calibrated in conjunction with the circuit testing.

Errors in the bipolar transistor model, nonideal op-amp characteristics such as finite gain and offset voltage, and process variations (both local and global) of resistor values cause errors in the voltage reference output. Resistor temperature dependencies and coefficient variations, Early voltage of the bipolar transistor, bipolar transistor emitter area mismatch, base spreading resistance, the temperature dependence of the transistor β, and package stress [22], [24] contribute to deviations in the reference output as well. Local and global variations in R_0, R_1, and R_2, in particular, will cause a significant change in performance and are often the dominant contributors to performance degradation [6].

Although calibration can significantly improve performance and a very high level of performance can be achieved with enough calibration points, the cost of calibration can be also be high when multiple calibration points or multiple calibration temperatures are required. From a practical viewpoint, there are very tight restrictions on the number of trim points and the number of trim temperatures that can be used.

5.1 Calibration

A standard method used in industry for trimming on-chip band gap reference circuits is termed a one-point trim. The one-point trim is done at the standard test temperature. In the one-point trim, R_0 often serves as the trimming resistor for the Kuijk structure [16], [6].

The goal with a one-point trim is to adjust the inflection point to be at the desired value and to have the output assume the desired value at the inflection point. There are three factors that make this difficult to achieve with a one-point trim. The inflection temperature and the output at the inflection temperature represent two degrees of freedom yet measurement of the output that can serves as input to the trim algorithm gives information at only a single temperature which is the trim temperatures. The third factor is due to the fact that the standard test temperature (which is also the trim temperature) is often different from the inflection temperature. These factors limit the performance after trimming.

A link-trim network is shown in Fig. 22 where the trimming elements are depicted as switches. Often the trimming elements will be metal interconnects that can be only opened during the trim.

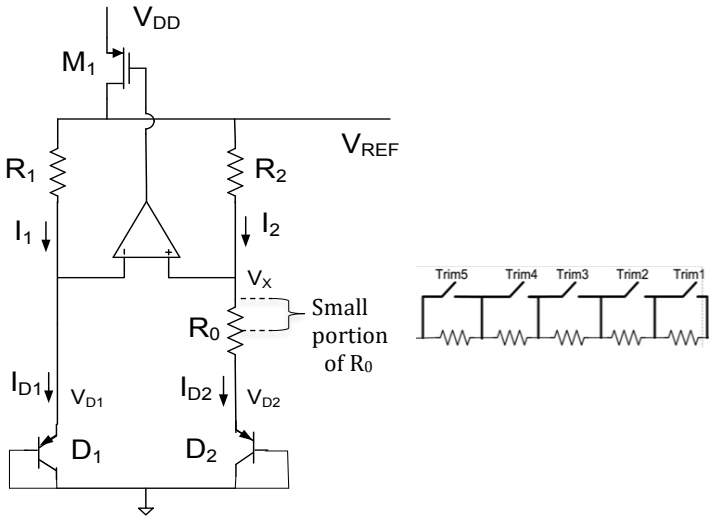


Figure 22 Schematic of the trimming resistor Ro

Fig. 23 shows the concept of using a single-point trim to trim both the inflection point and the value of the inflection point by trimming at a single temperature T_{TEST}. In the simulated trim shown in this figure it has been assumed that T_{TEST}=60°C and that the trimming resistor has infinite resolution. In the simulation depicted in the figure, it has been assumed that the bandgap reference is characterized by the analytical model of Sec. 2.2 that the reference output is given precisely by (33)-(36), and that a_1 in (34) and c_1 in (36) are equal to the desired values. Implicit in these assumptions is that the nonideal performance is due to errors in some parameters that determine b_1 in (35). To facilitate the trim, the resistor value R_0 was intentionally under-sized to guarantee that the untrimmed inflection point would be at a higher temperature than the desired inflection point. The trim algorithm was based upon measuring the output voltage at T_{TEST} and trimming R_0 through repeated measurements and R_0 trims (increases) until the output at T_{TEST} is equal to the desired value at T_{TEST}. It can be observed from this simulation that by trimming R_0 at the testing temperature, T_{INF} and $V_O(T_{INF})$ can be calibrated precisely to

the desired values. But the strict model assumptions that were made about the analytical model used in these simulations will invariably not be realized in a real circuit and if this happens, the inflection point and the value at the inflection point can differ considerably from when this single-point trim algorithm is used. These model errors can significantly degrade the TC of the trimmed reference. Industry will often use a minor variant to this single-point trim. Instead of trimming to the desired value at T_{TEST}, a set of reference output measurements will often be made on several test die at several different temperatures and then R_0 will be adjusted to an experimentally determined reference output at T_{TEST} that will result in the inflection point approximately assuming the desired value. But even with this approach, significant shifts in the actual inflection temperature often occur [6].

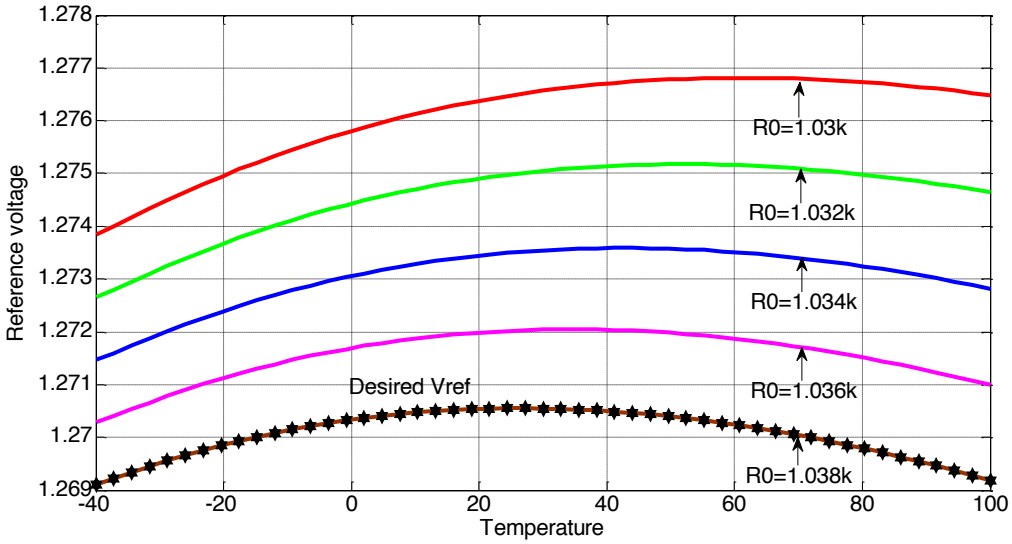


Figure 23 Calibration by trimming R_0

5.2 Voltage reference output after calibration

The number of resistor in series determines the resolution of the network. The trim will ideally adjust the inflection point to the desired location but since the trim is done at a single temperature, the actual position of the inflection point is not known. Alternatively, it is often assumed that if R_0 is trimmed so that the output assumes the ideal value at the trim temperature, then the inflection point will move to the desired value as well. This will occur if R_1 and R_2 remain matched and the errors are caused by an error in the ratio $\frac{R_1}{R_0}$.

Calibration is used to improve performance of the circuit after fabrication. It is impossible to cover all non-ideal effects that are introduced in the fabrication process by using a simulator. In this section, only process variations in the resistors R_0, R_1, and R_2 will be taken into consideration. More detailed investigations that include local random variations and other modeled parameters that are subject to variations as well as non-modeled parameters that can best be studied with fabricated test circuits will be left to future work.

Three different values for the resistor values, denoted as Typical, Corner 1, and Corner 2, are shown in Table 12. The two corners correspond to 20% process variations above and below the typical values.

Computer simulations will be investigate the effects of process variations on the performance of the bandgap circuit. Simulated results are based upon the Kuijk bandgap circuit shown in Fig. 5 that has a diode-connected BJT. In this investigation it will be

assumed that the op-amp is ideal. In these simulations, the simulation environment of Section 4.5 that includes the combined effects of the series base resistance, the base-spreading resistance, β, and the temperature dependence of these parameters will be adopted.

Fig. 24 and Fig. 25 show the voltage reference output before and after calibration respectively for typical and for the two corners of the resistance values. The results for the typical simulation are identical to those of Section 4.5. The calibration temperature was 30 °C and the output has been trimmed to the nominal value (1.279 V) at 30 °C, which includes the non-ideal characteristics of the BJT. The inflection point location and TC before and after calibration are included in Table 12. The one-point calibration removes the shift in the output that occurred at the calibration temperature but this one-point trim actually degrades the inflection point and the TC. Trims to a different value at the calibration temperature may favorably affect the TC and the inflection point but will not be investigated in this thesis.

Trimming can also provide some compensation for other nonideal effects such as errors in the resistor ratios due to local random variations, deviations in the temperature coefficients, deviations in the base spreading resistance characteristics, and nonideal effects in the operational amplifier. However, the single-point trim will usually not be effective at moving the inflection point to the desired temperature and will not compensate for the degradation in performance due to the large curvature in the vicinity of the inflection point.

Table 12 Simulation environments and results for calibration

	Tolerance of R_1	Tolerance of R_2	Tolerance of R_0	Inflection Point before calibration	TC before calibration	Inflection Point after calibration	TC after calibration
Typical	Typical	Typical	Typical	30 °C	37.4 ppm/°C	52 °C	43.4 ppm/°C
Corner 1	+20%	+20%	+20%	-26 °C	99.2 ppm/°C	-37°C	103.1 ppm/°C
Corner 2	-20%	-20%	-20%	75 °C	75.6 ppm/°C	83 °C	77.2 ppm/°C

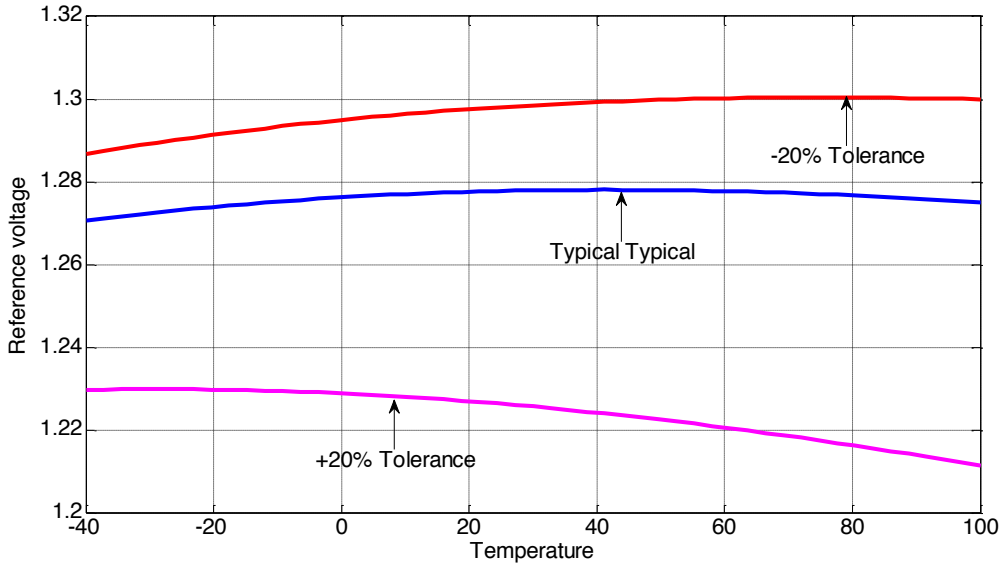


Figure 24 Voltage reference before calibration

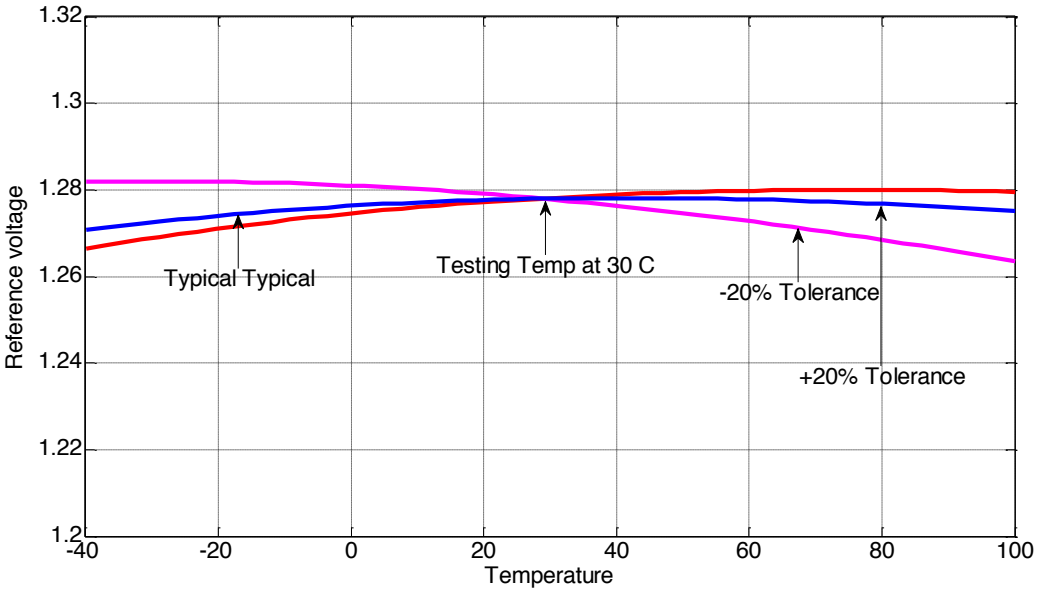


Figure 25 Voltage reference after calibration

CHAPTER 6: CONCLUSIONS

The effects of several non-ideal characteristics of the diode-connected substrate pnp bipolar transistor on the performance of bandgap circuits have been considered. Though the analysis was based upon the Kuijk reference, the methods are more generally applicable and the results will likely be similar for other bandgap circuits. In this analysis, major emphasis was placed on the base-spreading resistance of the substrate pnp bipolar transistor and on the temperature-dependence of the transistor current gain.

A multi-segment macro-model of a bipolar that incorporates the base spreading resistance and that can be used in standard circuit simulators was introduced. Though a large number of segments can improve accuracy, it was observed that in the applications considered in this work, little improvement in accuracy was obtained by using more than 8 segments in the macro-model.

Simulation results for a representative bandgap circuit designed in a 0.18 μm CMOS process show that the base spreading resistance dominantly causes a significant level shift in the output of the circuit and the temperature dependence of the current gain causes a significant shift in the inflection point. Both effects can contribute significantly to degradation in the temperature sensitivity of a bandgap reference.

For the specific implementation in a typical 0.18μm process of the bandgap circuit considered in this work, the base spreading resistance introduced a shift in the output voltage of about 6mV but caused little change in either the inflection point or the TC. The temperature dependence of the base spreading resistance also caused the voltage reference output to increase but had minimal effect on the inflection point. Neither the base

spreading resistance nor its temperature dependence caused a significant change in the TC of voltage reference.

The temperature dependence of the current gain of the bipolar transistor had a significant impact on the performance of the bandgap reference. The temperature dependence of β caused the inflection point of the voltage reference output to move to a much higher temperature. Without calibration, the shift in the inflection point due to the temperature dependence of β caused the TC to double. It is apparent that the temperature dependence of β can have a strong and adverse effect on the voltage reference in at least some semiconductor processes.

The temperature coefficient of the resistors in the Kuijk bandgap circuit also had a significant impact on the voltage reference output. They effected both the inflection point and the TC of the reference.

A single-temperature calibration algorithm was considered that focused only on calibrating for process variations in the resistor values of the Kuijk reference. It was shown that even with calibration, the residual inflection point errors can be significant and the TC can still be large.

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